WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a fin-shaped semiconductor layer which is formed on the semiconductor substrate, is long in a first direction and is short in a second direction crossing the first direction;

a gate insulating layer formed on side surfaces of the semiconductor layer in the second direction;

a gate electrode arranged so as to be adjacent to the gate insulating layer;

a channel area formed at a position adjacent to the gate insulating layer in the semiconductor layer;

a source/drain extension area which is formed at a position adjacent to the channel area in the semiconductor layer in the first direction; and

a source/drain area which is formed at a position adjacent to the source/drain extension area in the semiconductor layer in the first direction,

wherein a width of the semiconductor layer in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain area in the second direction.

2. The semiconductor device according to claim 1, wherein the width of the semiconductor layer in the channel area in the second direction is smaller than a width of the semiconductor layer in the source/drain

extension area in the second direction.

3. The semiconductor device according to claim 2, wherein the width of the semiconductor layer in the source/drain extension area in the second direction is smaller than the width of the semiconductor layer in the source/drain area in the second direction.

4. The semiconductor device according to claim 2, wherein the width of the semiconductor layer in the source/drain extension area in the second direction is equal to the width of the semiconductor layer in the source/drain area in the second direction.

5. The semiconductor device according to claim 1, wherein the width of the semiconductor layer in the channel area in the second direction is smaller than a gate length of the gate electrode.

6. The semiconductor device according to claim 1, wherein the width of the semiconductor layer in the source/drain extension area in the second direction is equal to or larger than a gate length of the gate electrode.

7. The semiconductor device according to claim 1, wherein the gate electrode is constituted by a first part which is formed on one side of the semiconductor layer in the second direction and a second part which is formed on the other side of the semiconductor layer in the second direction.

8. A semiconductor device comprising:

a semiconductor substrate;

a plurality of fin-shaped first semiconductor layers which are formed on the semiconductor substrate, long in a first direction, short in a second direction crossing the first direction, and aligned in the second direction;

a second semiconductor layer which connects a plurality of the first semiconductor layers with each other at end portions of a plurality of the first semiconductor layers in the first direction;

a gate insulating layer which is formed on side surfaces of each of a plurality of the first semiconductor layers in the second direction;

a gate electrode arranged so as to be adjacent to the gate insulating layer;

a channel area which is formed at a position adjacent to the gate insulating layer in a plurality of the first semiconductor layers;

a source/drain extension area formed at a position adjacent to the channel area in the first direction in a plurality of the first semiconductor layers; and

a source/drain area formed at a position adjacent to the source/drain extension area in the second semiconductor layer in the first direction.

9. The semiconductor device according to claim 8, wherein heights of a plurality of the first semiconductor layers are all equal to each other.

10. The semiconductor device according to claim 8, wherein the inside of the second semiconductor layer all consists of the source/drain area.

11. The semiconductor device according to claim 8, wherein a width of each of a plurality of the first semiconductor layers in the channel area in the second direction is smaller than a width of each of a plurality of the first semiconductor layers in the source/drain extension area in the second direction.

12. The semiconductor device according to claim 11, wherein the width of the first semiconductor layer in the source/drain extension area in the second direction is smaller than a width of the second semiconductor layer in the source/drain area in the second direction.

13. The semiconductor device according to claim 8, wherein the width of the first semiconductor layer in the channel area in the second direction is smaller than a gate length of the gate electrode.

14. A semiconductor device comprising:

a semiconductor substrate;

a fin-shaped semiconductor layer which is formed on the semiconductor substrate, is long in a first direction and is short in a second direction crossing the first direction;

a gate insulating layer formed on side surfaces of the semiconductor layer in the second direction;

a gate electrode arranged so as to be adjacent to the gate insulating layer;

a channel area formed at a position adjacent to the gate insulating layer in the semiconductor layer;

a source/drain extension area formed at a position adjacent to the channel area in the semiconductor layer in the first direction;

a source/drain area formed at a position adjacent to the source/drain extension area in the semiconductor layer in the first direction; and

a silicide layer which is formed on a surface portion of the semiconductor layer in the source/drain layer but not formed in the inner portion of the same.

15. The semiconductor device according to claim 14, wherein the silicide layer is formed on an upper portion of the semiconductor layer and a surface portion of the same in the second direction.

16. The semiconductor device according to claim 15, wherein an insulating layer which functions as a stopper in silicidation is formed between the silicide layer on the upper portion of the semiconductor layer and the semiconductor layer.

17. The semiconductor device according to claim 14, wherein a width of the semiconductor layer in the second direction is double-larger than a width of the silicide layer in the second direction which is formed on the surface portion of the semiconductor

layer in the second direction.

18. The semiconductor device according to claim 14, wherein a width of the semiconductor layer in the source/drain area in the second direction is larger than a width of the semiconductor layer in the source/drain extension area or the channel area in the second direction.

19. The semiconductor device according to claim 14, wherein a height of the semiconductor layer in the source/drain area is larger than a height of the semiconductor layer in the source/drain extension area or the channel area.

20. A manufacturing method of a semiconductor device comprising:

forming on a semiconductor layer a fin-shaped semiconductor layer which is long in a first direction and short in a second direction crossing the first direction;

forming a dummy gate insulating layer on side surfaces of the semiconductor layer in the second direction;

forming a dummy gate electrode adjacent to the dummy gate insulating layer;

forming a source/drain extension area and a source/drain area in the semiconductor layer;

forming an insulating layer which covers the semiconductor layer;

exposing surfaces of the dummy gate insulating layer and the dummy gate electrode by polishing or etching the insulating layer;

removing the dummy gate insulating layer and the dummy gate electrode;

oxidizing the semiconductor layer at a part where the dummy gate insulating layer had been formed, and forming an oxide layer there;

removing the oxide layer;

forming a gate insulating layer at a part where the dummy gate insulating layer had been formed; and

forming a gate electrode adjacent to the gate insulating layer.

21. A manufacturing method of the semiconductor device comprising:

forming on a semiconductor substrate a plurality of fin-shaped first semiconductor layers which are long in a first direction and short in a second direction crossing the first direction, and a second semiconductor layer which connects end portions of a plurality of the first semiconductor layers in the first direction with each other;

forming a dummy gate insulating layer on side surfaces of each of a plurality of the first semiconductor layers in the second direction;

forming a dummy gate electrode adjacent to the dummy gate insulating layer;

forming a source/drain extension area in each of a plurality of the first semiconductor layers;

forming a source/drain area in the second semiconductor layer;

forming an insulating layer which covers the first and second semiconductor layers;

exposing surfaces of the dummy gate insulating layer and the dummy gate electrode by polishing or etching the insulating layer;

removing the dummy gate insulating layer and the dummy gate electrode;

oxidizing the first semiconductor layer at a part where the dummy gate insulating layer had been formed, and forming an oxide layer there;

removing the oxide layer;

forming a gate insulating layer at a part where the dummy gate insulating layer had been formed; and

forming a gate electrode adjacent to the gate insulating layer.

22. A manufacturing method of a semiconductor device comprising:

forming a cap insulating layer on a semiconductor layer on a first insulating layer;

etching the semiconductor layer by using the cap insulating layer as a mask, and making the semiconductor layer into a fin shape which is long in a first direction and short in a second direction crossing the

first direction;

forming a second insulating layer which covers the semiconductor layer;

exposing a surface of the cap insulating layer by polishing or etching the second insulating layer;

reducing a size of the cap insulating layer by etching the cap insulating layer based on isotropic etching;

forming on the semiconductor layer a first resist having a slit whose width is smaller than a width of the semiconductor layer in the first direction;

making a width of the semiconductor layer at a central portion in the second direction smaller than a width of the semiconductor layer at an end portion in the first direction by etching the semiconductor layer with the cap insulating layer and the first resist being used as masks;

forming a source/drain extension area at the central portion of the semiconductor layer; and

forming a source/drain area at the end portion of the semiconductor layer in the first direction.

23. The manufacturing method according to claim 22, further comprising:

further reducing a size of the cap insulating layer by again etching the cap insulating layer based on the isotropic etching after etching the semiconductor layer with the cap insulating layer and the

resist being used as the masks and before forming the source/drain extension area;

forming on the semiconductor layer a second resist having a slit whose width is smaller than a width of the slit of the first resist in the first direction; and

making the width of the semiconductor layer at the central portion in the second direction smaller than the width of the semiconductor layer at the central portion in the second direction by etching the semiconductor layer with the cap insulating layer and the second resist being used as masks.

24. A manufacturing method of a semiconductor device comprising:

forming on a semiconductor layer a fin-shaped semiconductor layer which is long in a first direction and short in a second direction crossing the first direction;

forming a gate insulating layer on side surfaces of the semiconductor layer in the second direction;

forming a gate electrode adjacent to the gate insulating layer;

forming a source/drain extension area in the semiconductor layer by tilted ion implantation;

forming a sidewall insulating layer on a sidewall of the gate electrode;

forming a source/drain area by a combination of

tilted ion implantation and vertical ion implantation, or vertical ion implantation; and

forming a silicide layer on the gate electrode and a surface of the source/drain area,

wherein conditions of silicidation are set in such a manner the silicide layer is not formed in the entire inner portion of the semiconductor layer in the source/drain area.

25. A manufacturing method of a semiconductor device comprising:

forming on a semiconductor substrate a fin-shaped first semiconductor layer which is long in a first direction and short in a second direction crossing the first direction, a silicidation stopper on the first semiconductor layer, and a second semiconductor layer on the silicidation stopper;

forming a gate insulating layer on side surfaces of the first semiconductor layer in the second direction;

forming a gate electrode adjacent to the gate insulating layer;

forming a source/drain extension area in the first semiconductor layer;

forming a sidewall insulating layer on sidewalls of the gate electrode;

growing an epitaxial layer on surfaces of the first and second semiconductor layers by a selective

growth, and coupling the epitaxial layer from the first semiconductor layer with the epitaxial layer from the second semiconductor layer;

forming a source/drain area in the first semiconductor layer; and

forming a silicide layer on the gate electrode, the second semiconductor layer and the epitaxial layer,

wherein the silicidation stopper functions as a stopper in silicidation in such a manner that silicidation does not proceed from an upper portion of the first semiconductor layer in silicidation.

26. The semiconductor device according to claim 14, further comprising:

a sidewall insulating layer which covers a plurality of the first semiconductor layers to a boundary between the first and second semiconductor layers; and

a silicide layer which is formed by siliciding the second semiconductor layer,

wherein the second semiconductor layer has a square shape, and a width from an angular portion of a first semiconductor layer placed at a farthest end among a plurality of the first semiconductor layers to an angular portion of the second semiconductor layer is set larger than a thickness of the silicide layer.

27. The semiconductor device according to claim 26, wherein the silicide layer does not reach the

first semiconductor layer placed at the farthest end among a plurality of the first semiconductor layers.